

FIG-1

120 →

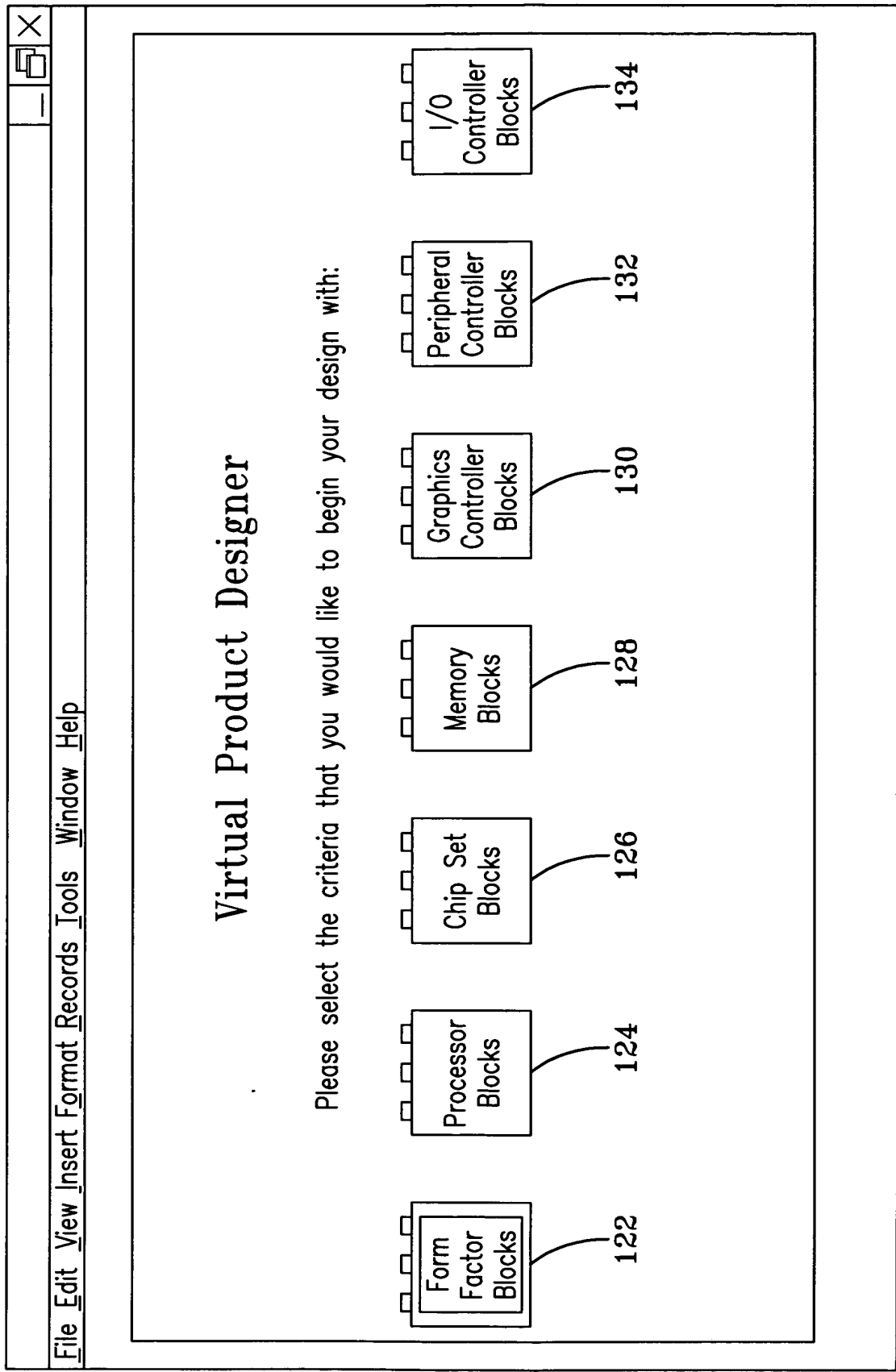
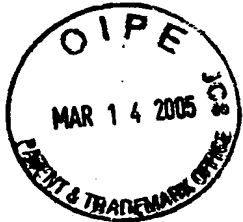


FIG-2



140

File Edit View Insert Format Records Tools Window Help	
Virtual Product Designer	
What is your form factor?	
<input type="checkbox"/> Baby AT <input type="checkbox"/> LPX <input type="checkbox"/> ATX <input type="checkbox"/> NLX <input type="checkbox"/> POS51 <input type="checkbox"/> cPCI <input type="checkbox"/> Custom	
<input type="button" value="Back"/> <input type="button" value="Done"/> <input type="button" value="Next >>"/>	
Features of Your Design	
Form Factor - Processor - Chip Set - Memory - Graphics Controller - Peripheral Controller - Controller -	
<u>YOUR DESIGN FEASIBILITY</u>	
<u>COMPONENT DENSITIES</u> Single sided assembly area _____ % Double sided assembly area _____ % Panel area used _____ %	
<u>POWER DISSIPATION</u> Worst case _____ W Typical _____ W	
<u>ESTIMATED COSTS 2500</u> Material _____ \$ Assembly labor _____ \$ Overhead and Profit _____ \$ Total estimated cost _____ \$ Production Lead-time _____ weeks	
Disclaimer Area	

146

148

144

FIG-3



150

Virtual Product Designer		YOUR DESIGN FEASIBILITY	
I/O Controllers?		COMPONENT DENSITIES	
<input type="checkbox"/> Super I/O Controller		Single sided assembly area	
<input type="checkbox"/> 10/100 Base-T Ethernet		Double sided assembly area	
<input type="checkbox"/> Serial I/O Ports		Panel area used	
<input type="checkbox"/> Digital I/O Ports			
<input type="checkbox"/> 1394 Interface		POWER DISSIPATION	
<input type="checkbox"/> GPS Interface		Worst case	
<input type="checkbox"/> Custom		Typical	
		ESTIMATED COSTS 2500	
<input type="button" value="Back"/> <input type="button" value="Done"/> <input type="button" value="Next =>"/>		Material	
Features of Your Design		Assembly labor	
Form Factor - Custom PCB 5.75 x 8.00 Panel 5.75 x 1.50		Overhead and Profit	
Processor - ABC 166 MHz		Total estimated cost	
Chip Set - DEF Chipset		Production Lead-time	
Memory - 32 MByte on board, no cache NVRAM socket			
Graphics Controller - XYZ Video, LCD Interface			
Peripheral Controller - IDE, Floppy, 2 DSB			
Controller - Super I/O, Ethernet			
		Disclaimer Area	

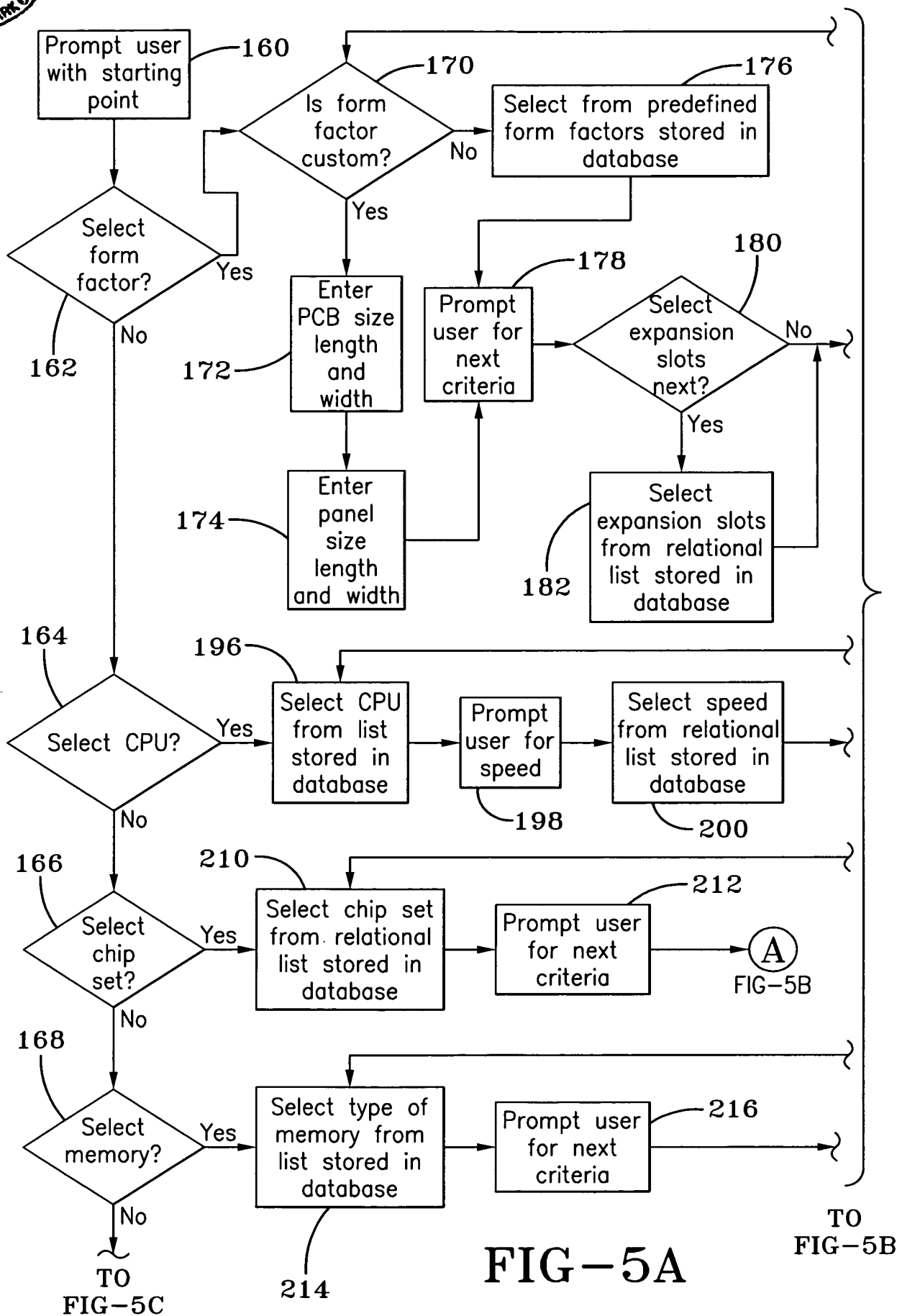
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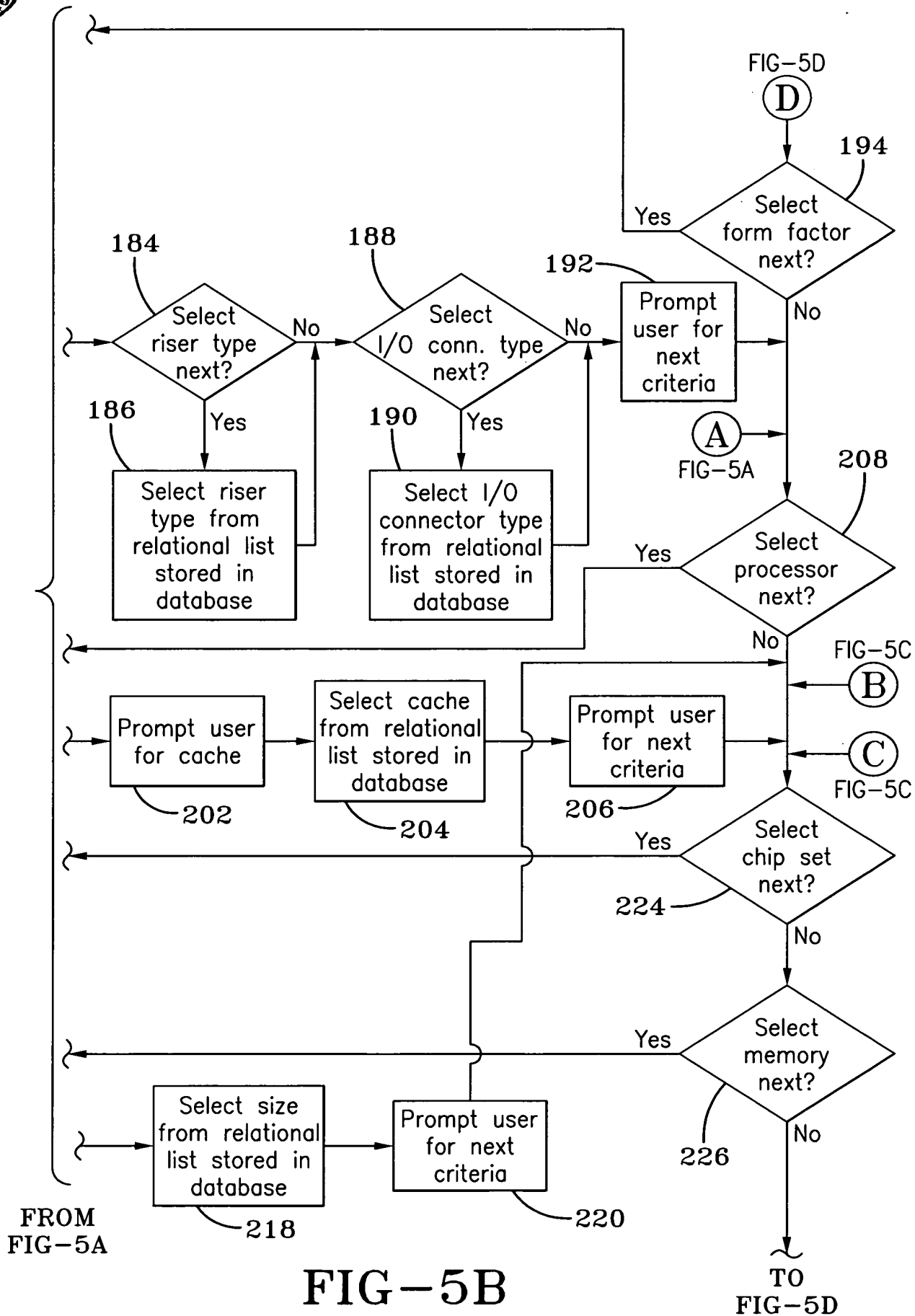
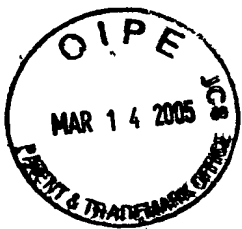
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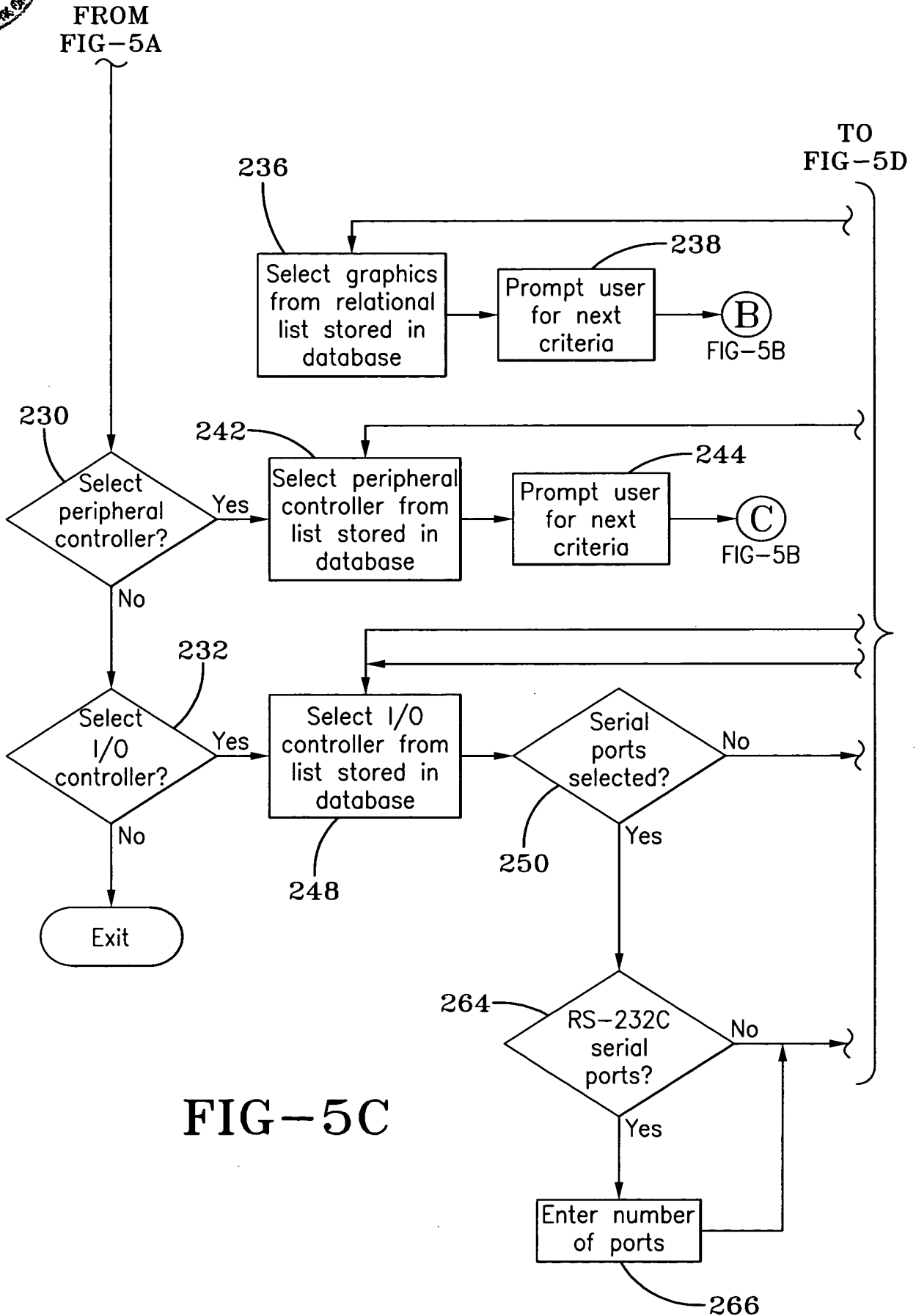
154

158

FIG-4







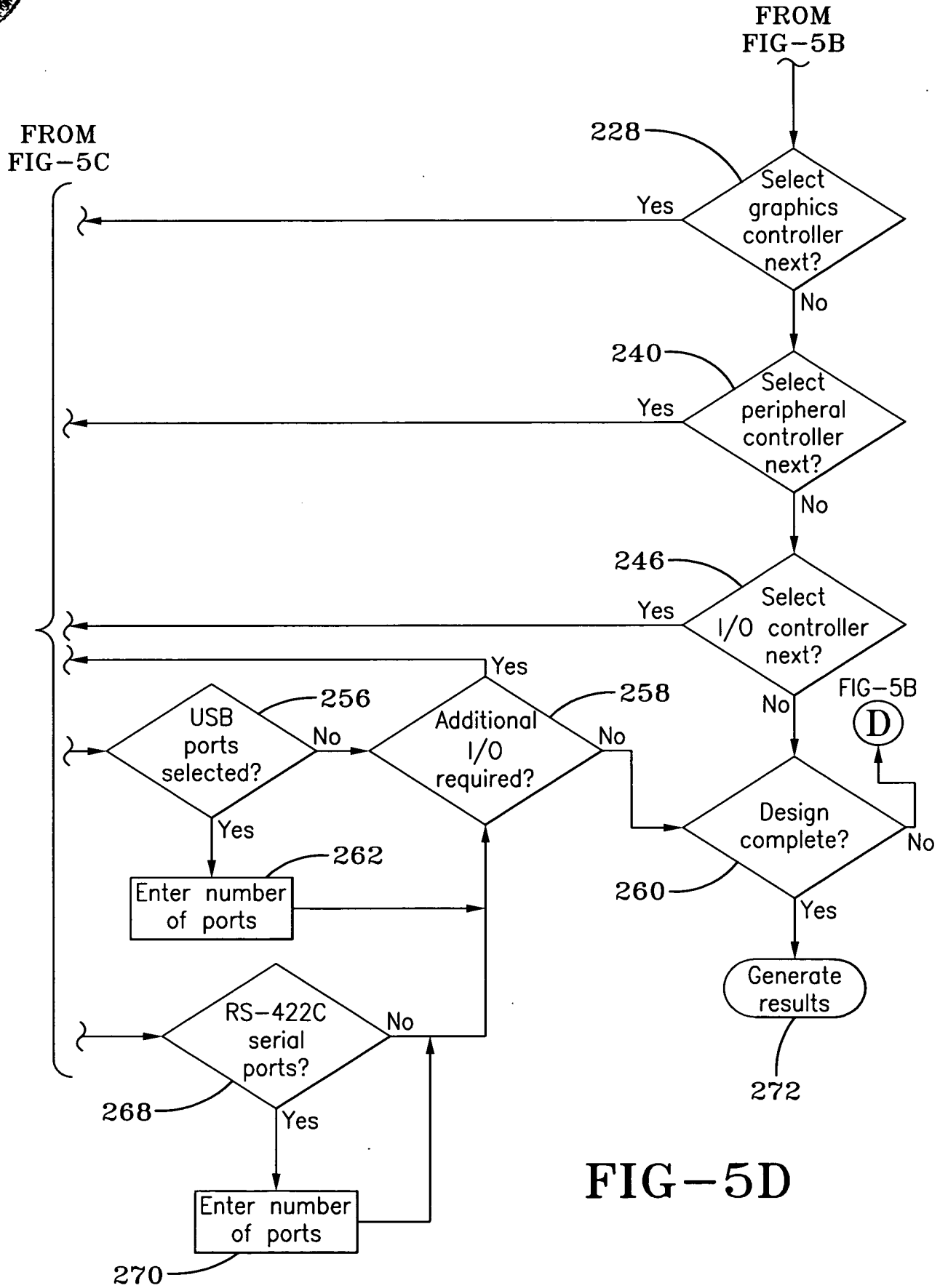


FIG-5D